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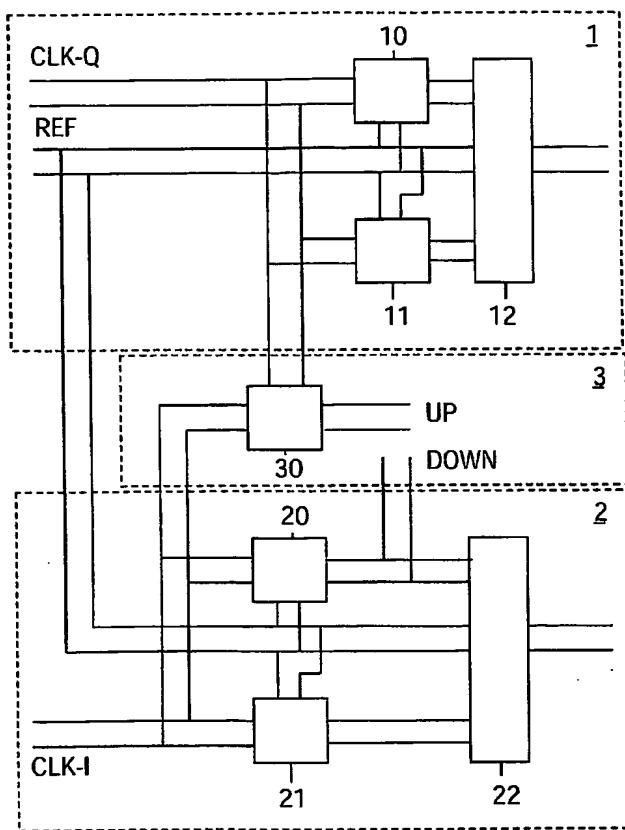
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(54) Title: FAST LINEAR PHASE DETECTOR



(57) Abstract: Linear phase detectors comprising circuits (1,2) receiving reference signals (REF) and first and second clock signals (CLK-Q, CLK-I) for generating first and second (phase) control signals (UP,DOWN) for use in multiplier circuits, demodulators and receivers, have large delays due to long path lengths and many operations between input and output (insight). They can be made faster by providing each circuit (1,2) with two parallel latches (10,11,20,21) and a multiplexer (12,22) for multiplexing latch output signals (basic idea). Said multiplexers generate (frequency control) signals to be supplied to frequency detectors, with a third circuit (3) generating at least one of said (phase) control signals (UP,DOWN). Said third circuit (3) comprises a latch (30) generating said first (phase) control signal (UP), with one of the latches (20) of the second circuit (2) generating the second (phase) control signal (DOWN). Or said third circuit (3) comprises logical circuitry (31-34) comprising four EXOR gates (31-34). A fifth EXOR gate (35) is used for balancing the third circuit (3).

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